Circuit Techniques for Clock Sources

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Almost all digital or communication systems require some form of clock source. Generating accurate and stable clock signals is often a difficult design problem.

Quartz crystals are the basis for most clock sources. The combination of high Q, stability vs time and temperature, and wide available frequency range make crystals a price-performance bargain. Unfortunately, relatively little information has appeared on circuitry for crystals and engineers often view crystal circuitry as a black art, best left to a few skilled practitioners (see box, "About Quartz Crystals").

In fact, the highest performance crystal clock circuitry does demand a variety of complex considerations and subtle implementation techniques. Most applications, however, don't require this level of attention and are relatively easy to serve. Figure 1 shows five (5) forms of simple crystal clocks. Types 1a through 1d are commonly referred to as gate oscillators. Although these types are popular, they are often associated with temperamental operation, spurious modes or outright failure to oscillate. The primary reason for this is the inability to reliably identify the analog characteristics of the gates used as gain elements. It is not uncommon in circuits of this type for gates from different manufacturers to produce markedly different circuit operation. In other cases, the circuit works, but is influenced by the status of other gates in the same package. Other circuits seem to prefer certain gate locations within the package. In consideration of these difficulties, gate oscillators are generally not the best possible choice in a production design; nevertheless, they offer low discrete component count, are used in a variety of situations, and bear mention. Figure 1a shows a CMOS Schmitt trigger biased into its linear region. The capacitor adds phase shift and the circuit oscillates at the crystal resonant frequency. Figure 1b shows a similar version for higher frequencies. The gate gives inverting gain, with the capacitors providing additional phase shift to produce oscillation. In Figure 1c, a TTL gate is used to allow the 10MHz operating frequency. The low input resistance of TTL elements does not allow the high value, single resistor biasing method. The R-C-R network shown is a

replacement for this function. Figure 1d is a version using two gates. Such circuits are particularly vulnerable to spurious operation but are attractive from a component count standpoint. The two linearly biased gates provide 360 degrees of phase shift with the feedback path coming through the crystal. The capacitor simply blocks DC in the gain path. Figure 1e shows a circuit based on discrete components. Contrasted against the other circuits, it provides a good example of the design flexibility and certainty available with components specified in the linear domain. This circuit will oscillate over a wide range of crystal frequencies, typically 2MHz to 20MHz.

The 2.2k and 33k resistors and the diodes compose a pseudo current source which supplies base drive.

At 25°C the base current is:

$$\frac{1.2V - 1V_{BE}}{33k} = 18\mu A$$

To saturate the transistor, which would stop the oscillator, requires V_{CE} to go to near zero. The collector current necessary to do this is:

$$IC(sat) = \frac{5V}{1k}(\text{delete } V_{CE} \text{ sat})$$
$$= 5mA$$

with 18μA of base drive a beta of:

$$\frac{5mA}{18\mu A} = 278 \text{ is required.}$$

At 1mA the DC beta spread of 2N3904's is 70 to ≅210.

The transistor should not saturate...even at supply voltages below 3V.

In similar fashion, the effects of temperature may also be determined.
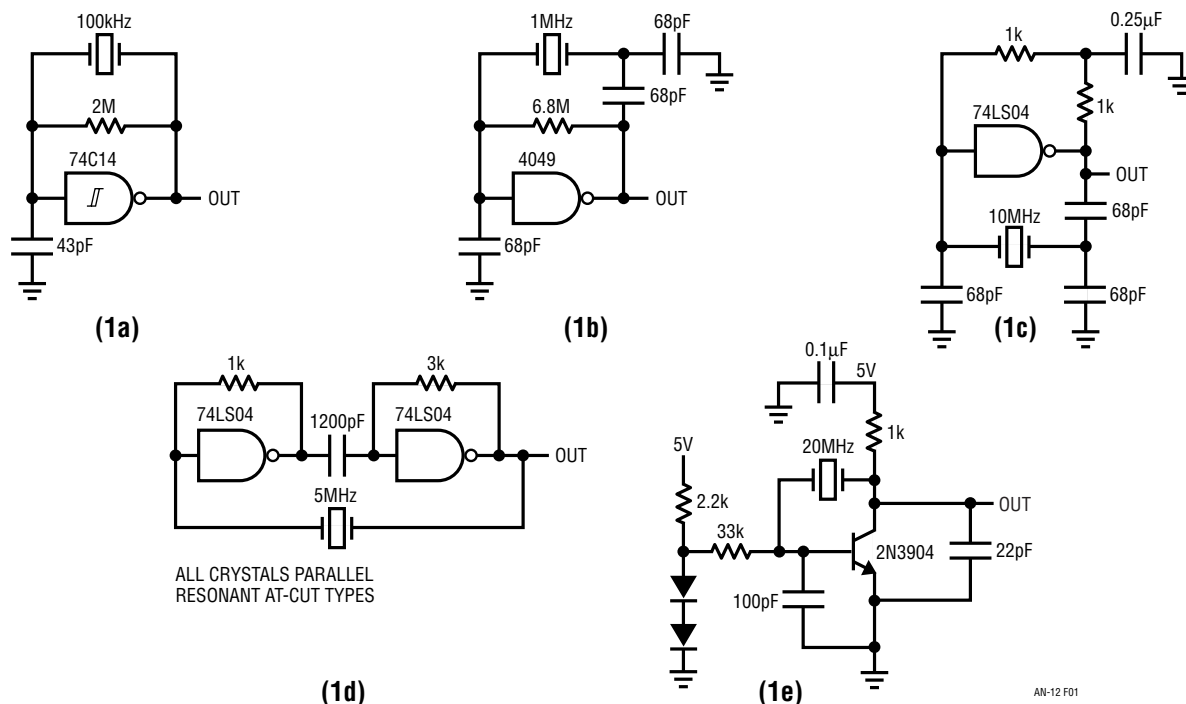
V_{BE} vs temperature over 25°C – 70°C is:

−2.2mV/°C • 45° = −99mV.

Figure 1. Typical Gate Oscillators and the Preferred Discrete Unit

The compliance voltage of the current source will move:

2 • –2.2mV/°C • 45°C = –198mV.

Hence, a first order compensation occurs:

–198mV – 99mV = –99mV total shift.

This remaining –99mV over temperature causes a shift in base current:

$$25°C \text{ current} = \frac{0.6V}{33k} = 18\mu A$$

$$70°C \text{ current} = \frac{0.5V}{33k} = 15\mu A$$

$$18\mu A – 15\mu A = 3\mu A$$

This 3μA shift (about 16%) provides a compensation for transistor h_{FE} shift with temperature, which moves about 20% from 25°C to 70°C. Thus the circuit's behavior over temperature is quite predictable. The resistor, diode and V_{BE} tolerances mean that only first order compensations for V_{BE} and h_{FE} over temperature are appropriate.

Figure 2 shows another approach. This circuit uses a standard RC-comparator multivibrator circuit with the crystal connected directly across the timing capacitor.

Because the free running frequency of the circuit is close to the crystal's resonance, the crystal "steals" energy from the RC, forcing it to run at the crystal's frequency. The crystal activity is readily apparent in Trace A of Figure 3, which is the LT[®]1011's "–" input. Trace B is the LT1011's output. In circuits of this type, it is important to ensure that enough current is available to quickly start the crystal resonating while simultaneously maintaining an RC time constant of appropriate frequency. Typically, the free running frequency should be set 5% to 10% above crystal resonance with a resistor feedback value calculated to allow about 100μA into the capacitor-crystal network. This type of circuit is not recommended for use above a few hundred kHz because of comparator delays.
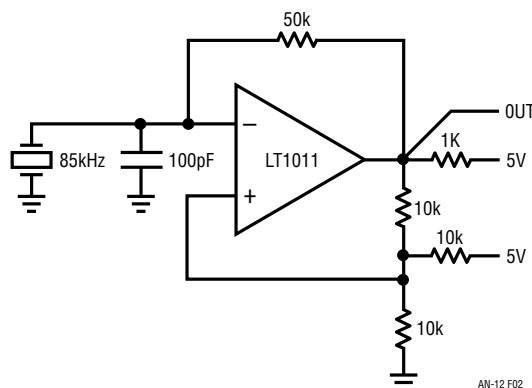

Figure 2. Crystal Stabilized Relaxation Oscillator

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Figures 4a and 4b use another comparator based approach. In Figure 4a, the LT1016 comparator is set up with DC negative feedback. The 2k resistors set the common mode level at the device's positive input. Without the crystal, the circuit may be considered as a very wideband (50GHz GBW) unity gain follower biased at 2.5V. With the crystal inserted, positive feedback occurs and oscillation commences. Figure 4a is useful with AT-cut fundamental mode crystals up to 10MHz. Figure 4b is similar, but supports oscillation frequencies to 25MHz. Above 10MHz,

AT-cut crystals operate in overtone mode. Because of this, oscillation can occur at multiples of the desired frequency. The damper network rolls off gain at high frequency, insuring proper operation.

All of the preceding circuits will typically provide temperature coefficients of 1ppm/°C with long term (1 year) stability of 5ppm to 10ppm. Higher stability is achievable with more attention to circuit design and control of temperature. Figure 5 shows a Pierce class circuit with fine frequency trimming provided by the paralleled fixed and
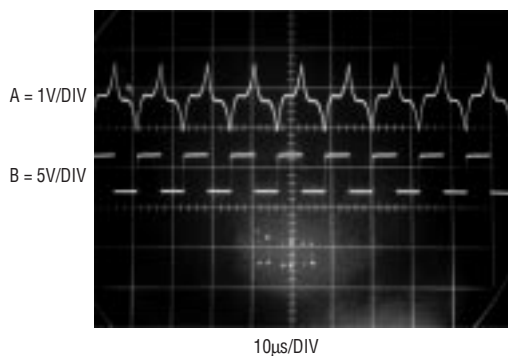

A = 1V/DIV

B = 5V/DIV

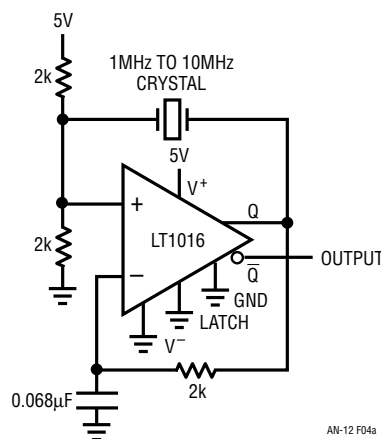10μs/DIV

Figure 3. Figure 2's Waveforms

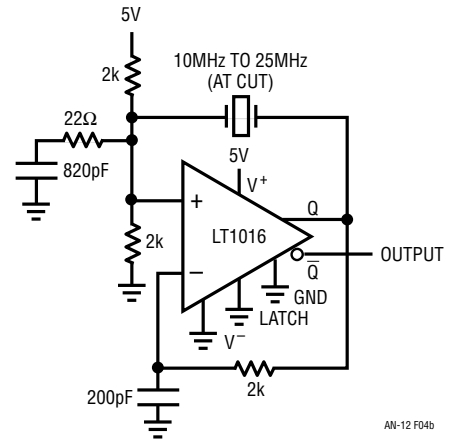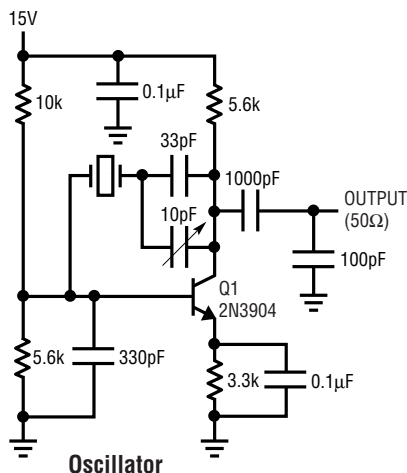**Figure 4a. 1MHz to 10MHz Crystal Oscillator**

Figure 4b. 10MHz to 25MHz Crystal Oscillator

Oscillator

* TRW MAR-6 RESISTOR

R_T = YELLOW SPRINGS INST. #44014 75°C = 35.39k
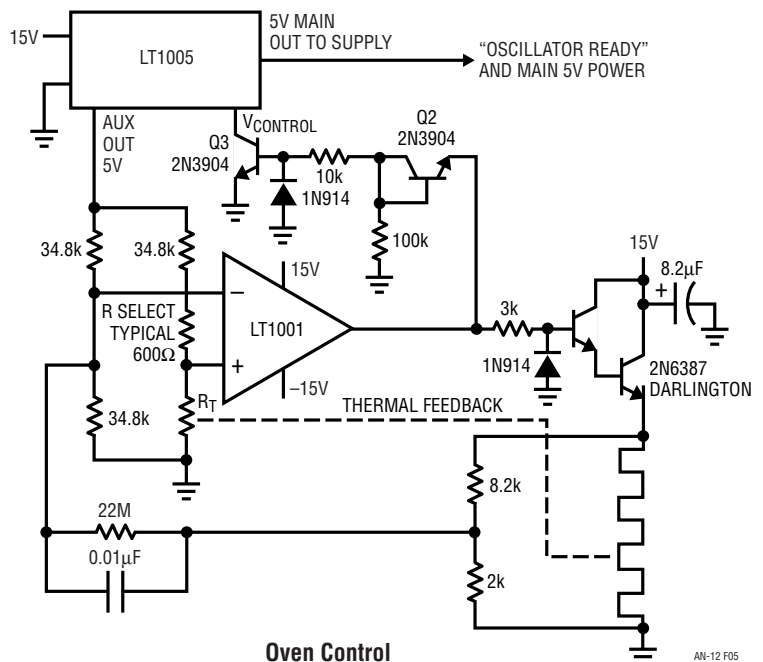
⊟ = BLILEY #BG61AH-55, 75°C TURNING POINT. 5MHz FREQUENCY

Oven Control

Figure 5. Ovenized Oscillator

variable capacitors. The transistor provides 180° of phase shift with the loop components adding another 180°, resulting in oscillation. The LT1005 voltage regulator and the LT1001 op amp are used in a precision temperature servo to control crystal temperature. The LT1001 extracts the differential bridge signal and drives the Darlington stage to power the heater, which is monitored by the thermistor. In practice, the sensor is tightly coupled to the heater. The RC feedback values should be optimized for the thermal characteristics of the oven. In this case, the oven was constructed of aluminum tube stock 3" long × 1" wide × 1/8" thick. The heater windings were distributed around the cylinder and the assembly placed within a small insulating Dewar flask. This allows 75°C setpoint (the zero TC or "turnover" temperature of the crystal specified) control of 0.05°C over 0°C to 70°C. The LT1005 regulator sources bridge drive from its auxiliary output and also keeps system power off until the crystal's temperature (hence, its frequency) is stabilized. When power is applied the negative TC thermistor is high in value, causing the LT1001 to saturate positive. This turns on zener-connected Q2, biasing Q3. Q3's collector current pulls the regulator's control pin low, disabling its output. When the oven arrives at its control point, the LT1001's output comes out of saturation and servo controls the oven at a point well below Q2's zener value. This turns off Q3, enabling the regulator to source power to whatever system the clock is associated with. For the crystal and circuit values specified, this clock will drift less than 1×10^{-9} over 0°C to 70°C with a time drift of 1 part 10^{-9} week.

The oven approach to removing temperature effects of crystal clock frequency is the most effective and in wide use. Ovens do, however, require substantial power and warm-up time. In some situations, this is unacceptable. Another approach to offsetting temperature effects is to measure ambient temperature and insert a scaled compensation factor into the crystal clock's frequency trimming network. This open loop correction technique relies on matching the clock frequency vs temperature characteristic, which is quite repeatable. Figure 6 shows a temperature compensated crystal oscillator (TXCO) which uses a first order linear fit to correct for temperature. The oscillator is a Colpitts type, with a capacitive tapped tank network. The LT319A picks off the output and the RC network at the LT319's "–" input provides a signal adaptive trip threshold. The LT1005 regulator's auxiliary output buffers supply variations and the main regulator output control pin allows the system to be shut down without removing power from the oscillator, aiding overall stability. The ambient temperature is sensed by the linear thermistor network in A1's feedback loop with A2 used for scaling and offsetting. A2's voltage output expresses the
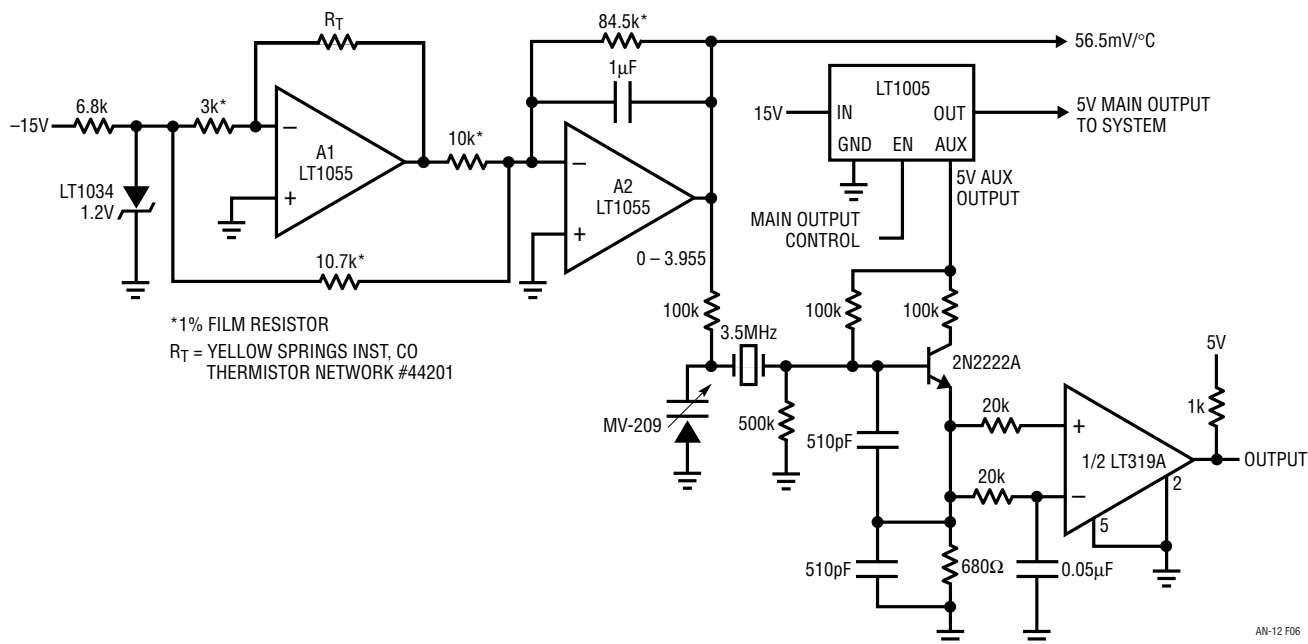

Figure 6. Temperature Compensated Crystal Oscillator (TXCO)

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ambient temperature information required to compensate the clock. The correction is implemented by biasing the varactor diode (a varactor diode's capacitance varies with reverse bias) which is in series with the crystal. The varactor's shift in capacitance is used to pull the crystal's frequency in a complementary fashion to the circuit's temperature error. If the thermistor is maintained isothermally with the circuit, compensation is very effective. Figure 7 shows the results. The –40ppm frequency shift over 0°C to 70°C is corrected to within 2ppm. Better compensation is achievable by including 2nd and 3rd order terms in the temperature to voltage conversion to more accurately complement the nonlinear frequency drift characteristic.

Figure 8 is another voltage-varactor tuned circuit but is configured to allow frequency shift instead of opposing it. This voltage controlled crystal oscillator (VXCO) has a

clean 20MHz sine wave output (Figure 9) suitable for communications applications. The curve of Figure 10 shows a 7kHz shift from 20MHz over the 10V tuning range. The 25pF trimmer sets the 20MHz zero bias frequency. In many applications, such as phase-locking and narrow bandwidth FM secure communications, the nonlinear response is irrelevant. Improved linearity will require conditioning the tuning voltage or the varactor network's response. In circuits of this type it is important to remember that the limit on pulling frequency is set by the crystals Q, which is high. Achieving wide dynamic "pull" range without stopping the oscillator or forcing it into abnormal modes is difficult. Typical circuits, such as this one, offer pull ranges of several hundred ppm. Larger shifts (e.g., 2000ppm to 3000ppm) are possible without losing crystal lock, although clock output frequency stability suffers somewhat.
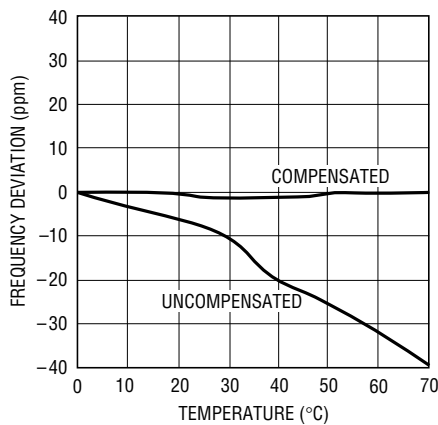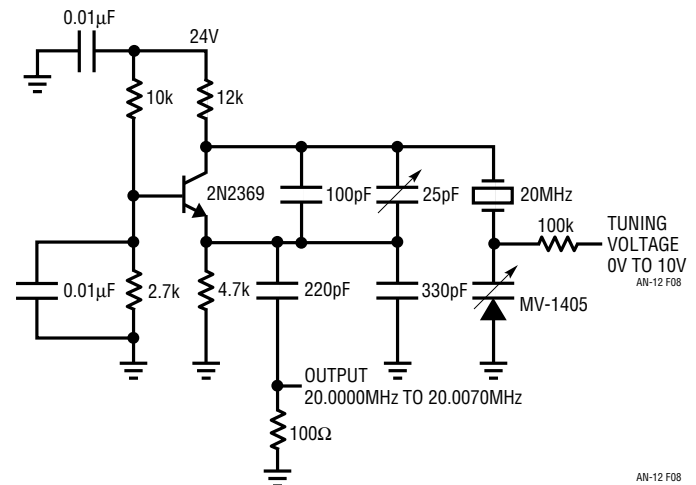

Figure 7. TXCO Drift Performance

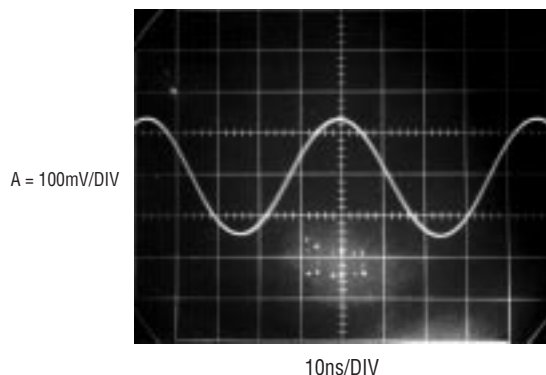Figure 8. Voltage Controlled Crystal Oscillator (VCXO)

Figure 9. Figure 8's Output
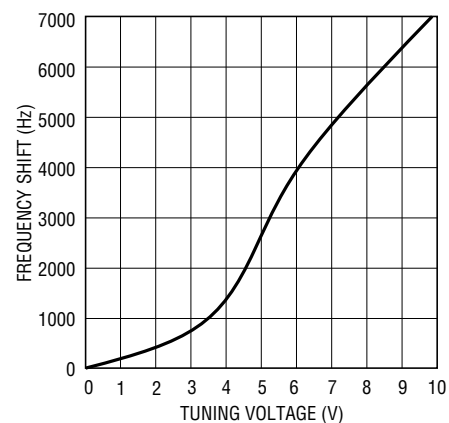

Figure 10. Figure 8's Tuning Characteristics

Noncrystal Clock Circuits

Although crystal based circuits are universally applied, they cannot serve all clock requirements. As an example, many systems require a reliable 60Hz line synchronous clock. Zero crossing detectors or simple voltage level detectors are often employed, but have poor noise rejection characteristics. The key to achieving a good line clock under adverse conditions is to design a circuit which takes advantage of the narrow bandwidth of the 60Hz fundamental. Approaches utilizing wide gain bandwidth, even if hysteresis is applied, invite trouble with noise. Figure 11 shows a line synchronous clock which will not lose lock under noisy line conditions. The basic RC multivibrator is tuned to free run near 60Hz, but the AC-line derived synchronizing input forces the oscillator to lock to the line. The circuit derives its noise rejection from the integrator characteristics of the RC network. As Figure 12 shows, noise and fast spiking on the 60Hz input (Trace A, Figure 12) has little effect on the capacitor's charging characteristics (Trace B, Figure 12) and the circuit's output (Trace C, Figure 12) is stable.
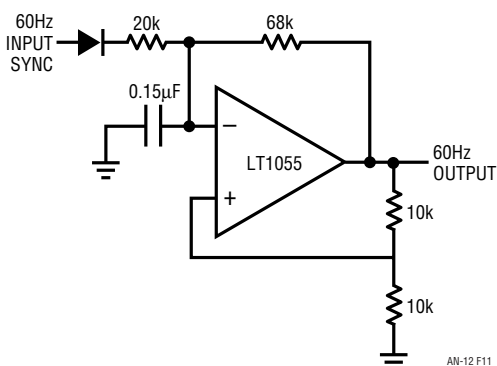
Figure 13 is another synchronous clock circuit. In this instance, the circuit output locks at a higher frequency than the synchronizing input. Circuit operation is the time domain equivalent of a reset stabilized DC amplifier. The LT1055 and its associated components form a stable oscillator. The LM329 diode bridge and compensating diodes provide a stable bipolar charging source for the RC located at the amplifier's negative input. The synchronizing pulse (Trace A, Figure 14) is level shifted by the LT1011 comparator to drive the FET. When the synchronizing pulse appears, the FET turns on, grounding the capacitor (Trace B, Figure 14). This interrupts normal oscillator action, but only for a small fraction of a cycle. When the sync pulse falls, the capacitor's charge cycle, which has been reset to 0V, starts again. This resetting action forces the frequency of the RC charging to be synchronous and stabilized by the sync pulse. The only evidence of this operation at the output is an occasional, slightly enlarged pulse width (Trace C, Figure 14), which is caused by the synchronizing interval. The sync adjust potentiometer
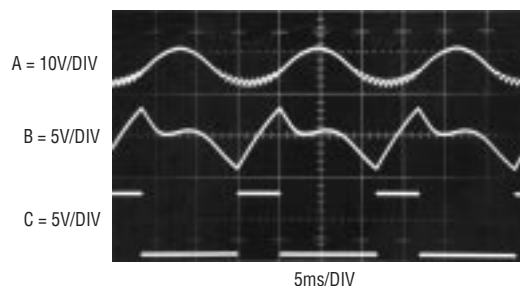

Figure 11. Synchronized Oscillator

Figure 12. Figure 11's Waveforms

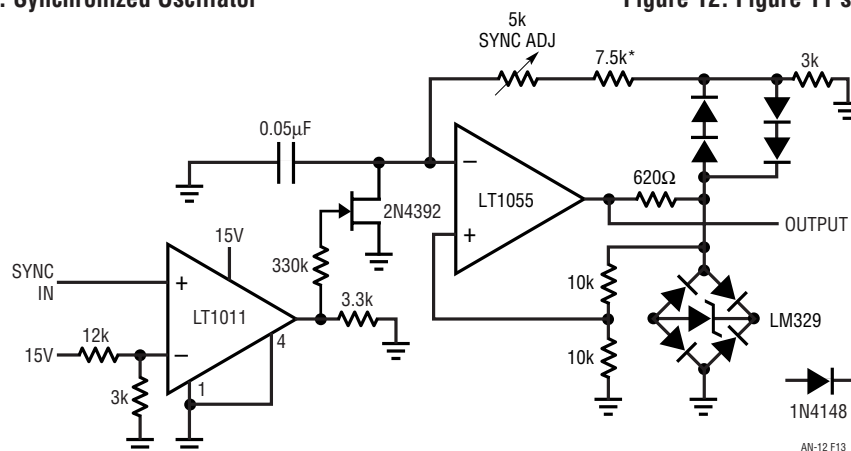**Figure 13. Reset Stabilized Oscillator**

should be trimmed so the sync pulse appears when the capacitor is near 0V. This minimizes output waveform width deviation and allows maximum protection against losing lock due to RC drift over time and temperature. The maximum practical output frequency to sync frequency ratio is about 50×.

Pure RC oscillators are a final form of clock circuit. Although this class of circuit cannot achieve the stability of a synchronized or crystal based approach, it offers simplicity, economy and direct low frequency output. As such they are used in baud rate generators and other low frequency applications. The key to designing a stable RC oscillator is to make output frequency insensitive to drift in as many circuit elements as possible. Figure 15 shows an RC clock circuit which depends primarily on the RC elements for stability. All other components contribute very low order error terms, even for substantial shifts. In addition, the RC components have been chosen for opposing temperature coefficients, further aiding stability. The circuit is a standard comparator-multivibrator with parallel CMOS inverters interposed between the comparator output and the feedback resistors. This replaces the relatively large and unstable bipolar V_{CE} saturation losses of the LT1011 output with the superior ON characteristics

of MOS. Not only are the MOS switching losses to the rails low and resistive, but they tend to cancel. The paralleling of inverters further reduces errors to insignificant levels. With this arrangement, the charge and discharge time constant of the capacitor is almost totally immune from supply and temperature shifts. The 10k units need not be precision types, because shifts in them will cancel. In addition, the effect of the comparator's DC input errors is also negated because of the symmetrical nature of the oscillator. This leaves only the RC network as a significant error term. The nominal—120ppm/°C temperature coefficient of the polystyrene capacitor is partially offset by the opposing positive temperature coefficient designed into the specified resistor. In practice, only a first order compensation is achievable because of the uncertainty of the capacitor's exact TC. For the test circuit, 0°C to 70°C temperature excursion showed a 15ppm/°C TC with a power supply rejection factor of less than 20ppm/V. In contrast, a clock constructed from the popular 555 timer, using the compensating RC network, showed 95ppm/°C and 1050ppm/V of supply shift. Because of comparator propagation delays, circuits of this type are less stable above a 5kHz to 10kHz operating frequency.
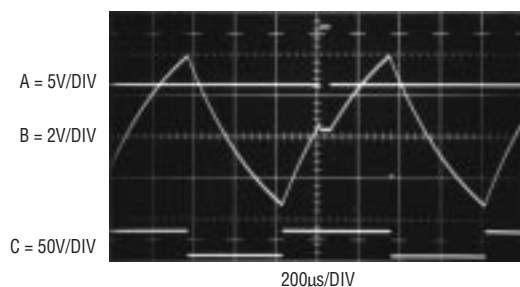

A = 5V/DIV

B = 2V/DIV

C = 50V/DIV

200µs/DIV

Figure 14. Figure13's Waveforms

74C04s

OUTPUT

C
0.015µF

15V

4.7k

LT1011

10k

10k 15V

10k

*TRW TYPE MTR-5/+120ppm/°C
C = 0.015µF = POLYSTYRENE—
120ppm/°C ±30ppm WESCO TYPE 32-P

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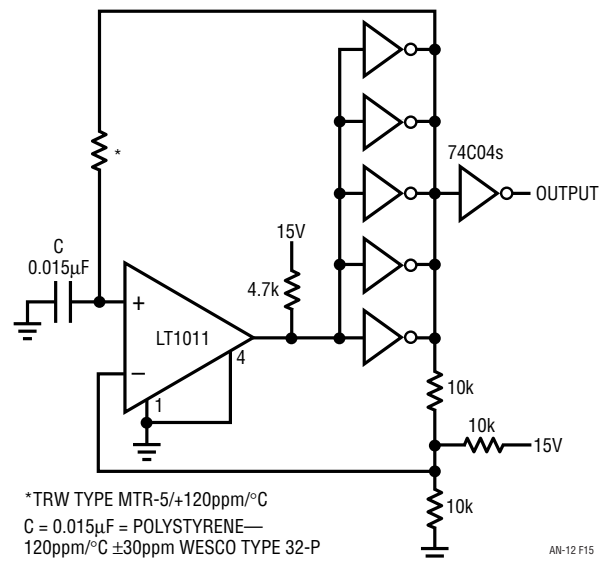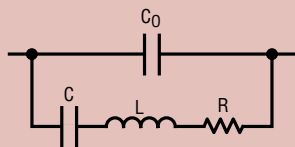**Figure 15. Stable RC Oscillator**

ABOUT QUARTZ CRYSTALS

The frequency stability and repeatability of quartz crystals represent one of nature's best bargains for the circuit designer. The equivalent circuit of a crystal looks like a series-parallel combination of elements.

Typical Values:

$R = 100\Omega$

$L = 500\mu H$

$C = 0.01pF$

$C_O = 5pF$

$Q = 50,000$

C_O is the static capacitance produced by the contact wires, crystal electrodes and the crystal holder. The RLC term is called the motional arm. C is the mechanical mass. R includes all electrical losses in the crystal and L is the reactive component of the quartz. Different angles of cut from the mother crystal produce different electrical characteristics in individual crystals. Cuts can be optimized for temperature coefficient, frequency range and other parameters. The basic "AT" cut used in most crystals in the 1MHz to 150MHz range is a good compromise between temperature coefficient, frequency range, ease of manufacture and other considerations. Other factors affecting resonator performance include the method of lead attachment, package sealing method and internal environment (e.g., vacuum, partial pressure, etc.). Some circuit considerations when using crystals include:

Load Capacitance—The reactance the crystal must present to the circuit. Some circuits use the crystal in the parallel resonant mode (e.g., the crystal looks inductive). Other circuits are specified as series resonant and the crystal appears resistive. In this mode, the circuit's load capacitance, including all parasitics, must be specified. A typical number is around 30pF.

Resistance—The impedance the crystal presents when it is resonating.

Drive Level—How much power may be dissipated in the crystal and still maintain all specifications. 10mW is typical. Excessive levels can fracture the crystal.

Temperature Coefficient/Turning Point—The tempco of the crystal is usually specified near the "turning point." This is the temperature at which the crystal tempco is zero. Typically the tempco will be below 1ppm/°C over the operating range and the turning point around 75°C, although different cuts can considerably alter these numbers.

Frequency Tolerance—The deviation from ideal frequency when used under specified circuit conditions at a defined temperature. Tolerances vary from 50ppm to less than 1ppm.

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